Clocked Cascade Voltage Switch Logic (C^2VSL) Adders

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ABSTRACT

A static cascade voltage switch logic (CVSL) half adder, a clocked cascade voltage switch logic (C^2VSL) half adder and a C^2VSL full adder have been originally and successfully designed and fabricated using a double polysilicon and double metal 1.2 μm CMOS technology. The three different adders have confirmed to function correctly by SPICE simulations. Furthermore, the fabricated three different adders have confirmed to function correctly by chip measurements.

1. INTRODUCTION

In the galactic cosmic ray environment typical of high altitude satellite orbits, a single event upset (SEU), which occurs when a charged particle passing through a cell deposits enough energy for the cell to change its state, should be taken into account. In order to design radiation-hardened LSIs for space applications, static cascade voltage switch logic (CVSL) circuits and clocked CVSL circuits were proposed by H. Hatano [1]-[5]. The CVSL circuit is a differential style of logic requiring both true and complement signals to gates. The CVSL has two storage nodes for each gate instead of one, resulting in higher tolerance of SET pulses than CMOS.

A static cascade voltage switch logic (CVSL) half adder, a clocked cascade voltage switch logic (C^2VSL) half adder and a C^2VSL full adder have been designed and fabricated using a double polysilicon and double metal 1.2 μm CMOS technology [6], [7].

2. CIRCUIT DESIGNS

2.1 Static CVSL Half Adder

A static CVSL half adder circuit diagram is shown in Fig. 1. Fig. 2 shows the static CVSL half adder layout. Simulation results is shown in Fig. 3, indicating that the designed static CVSL half adder functions correctly.

2.2 Clocked CVSL (C^2VSL) Half Adder

A C^2VSL half adder circuit diagram is shown in

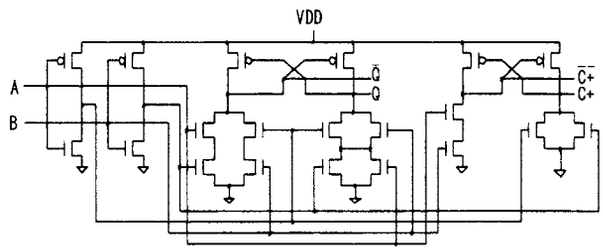

Fig. 1 Static CVSL half adder circuit diagram.

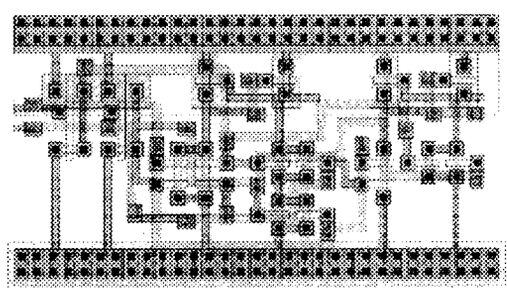

Fig. 2 Static CVSL half adder layout diagram.

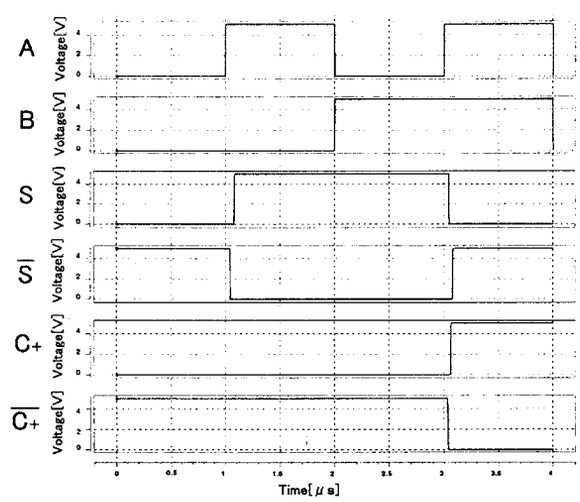

Fig. 3 Simulation waveforms of static CVSL half adder.

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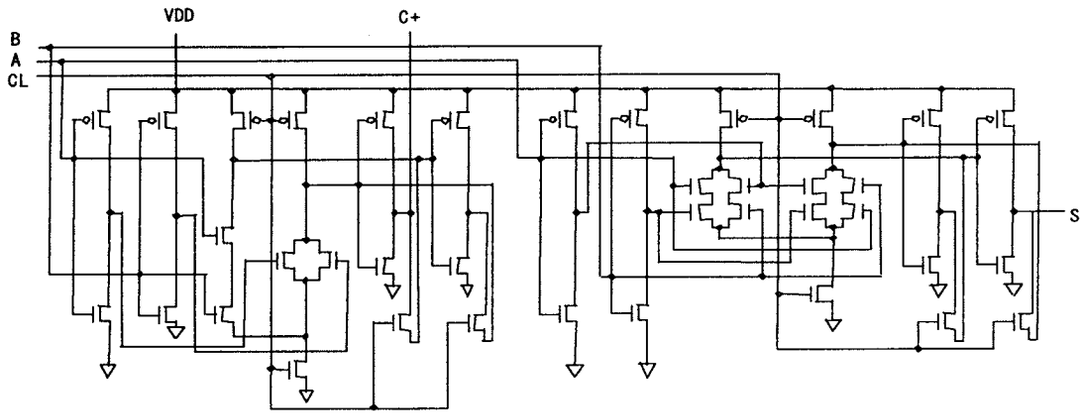

Fig. 4 C^2VSL half adder circuit diagram.

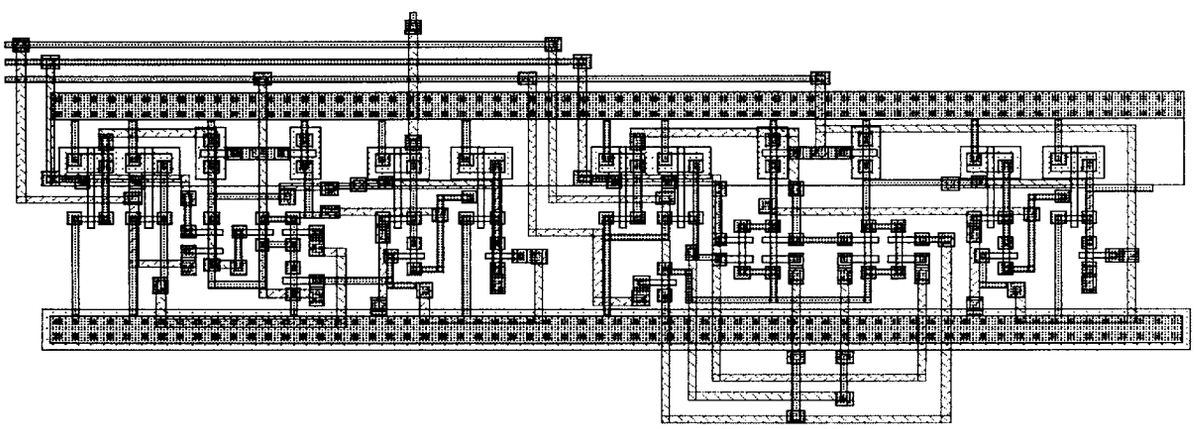

Fig. 5 C^2VSL half adder layout diagram.

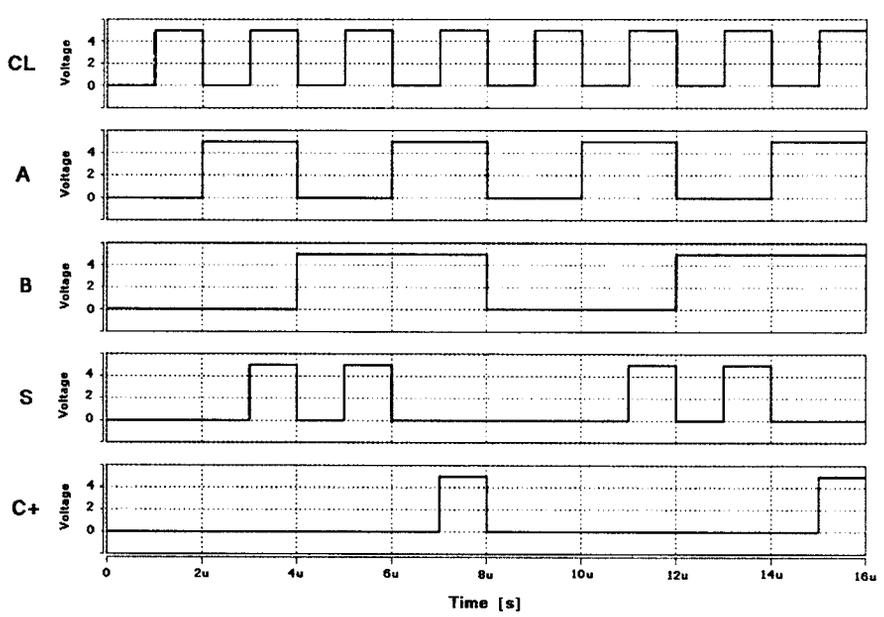

Fig. 6 Simulation waveforms of C^2VSL half adder.

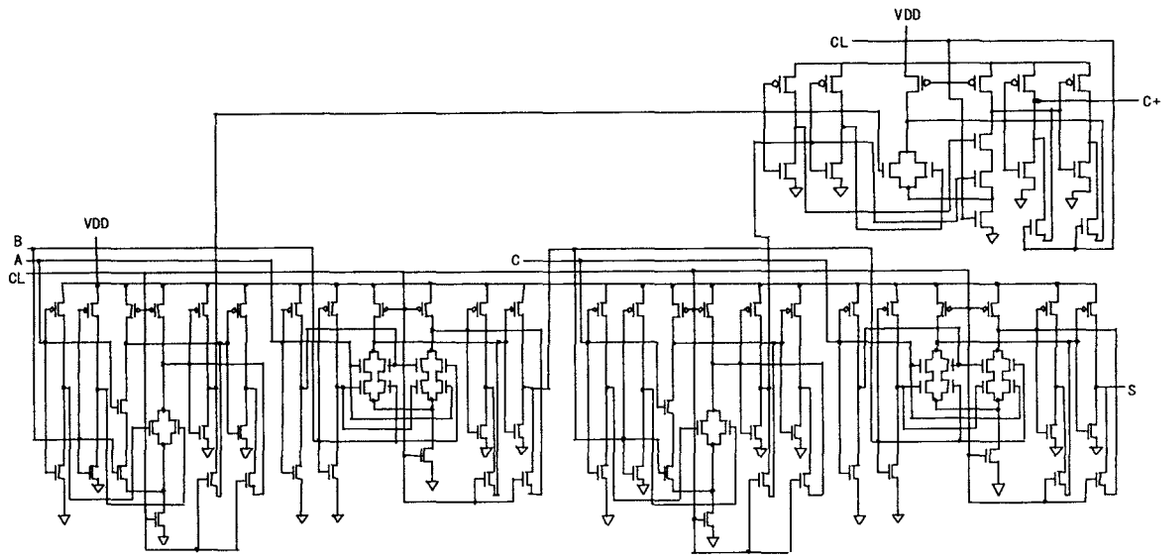

Fig. 7 C^2VSL full adder circuit diagram.

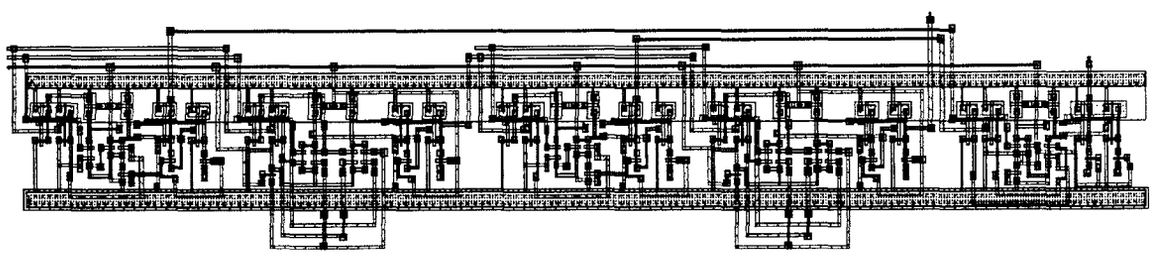

Fig. 8 C^2VSL full adder layout diagram.

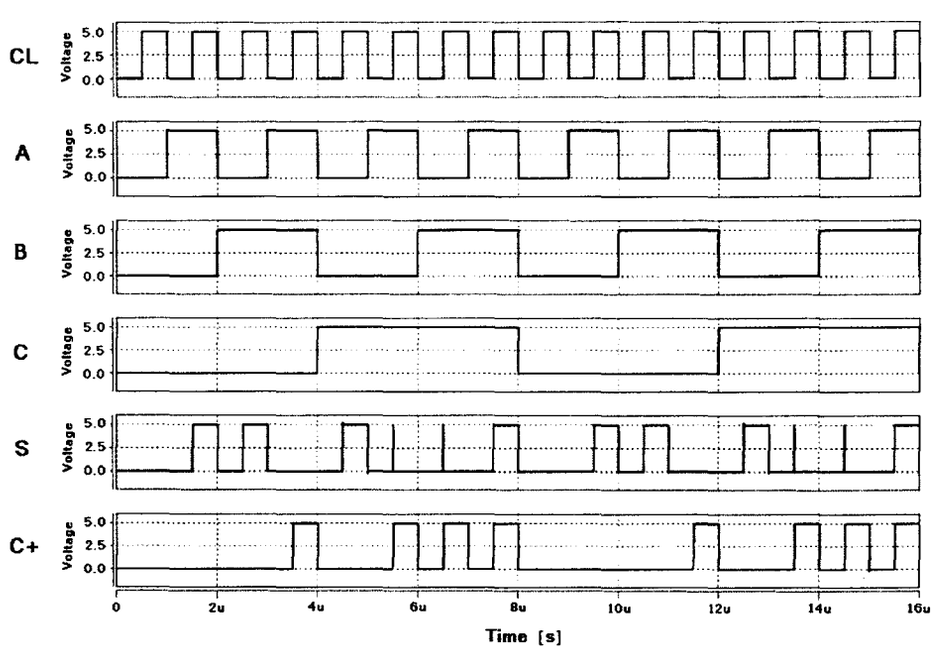

Fig. 9 Simulation waveforms of C^2VSL full adder.

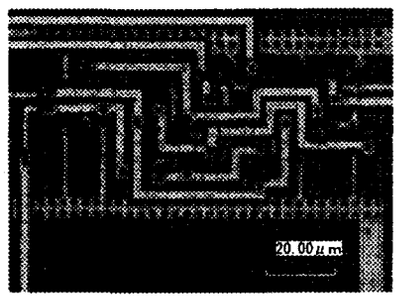

Fig. 10 Photomicrograph of fabricated static CVSL half adder.

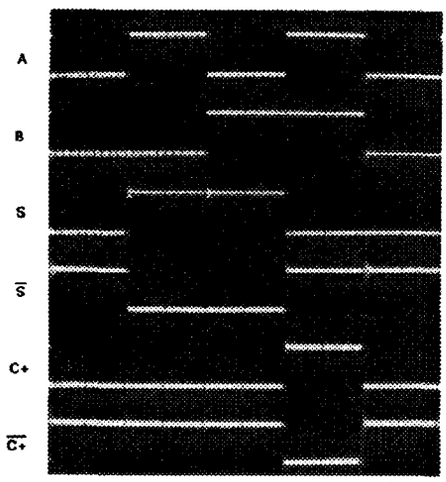

Fig. 11 Measured signal waveforms of static CVSL half adder. Horizontal axis: 5μs/div. Vertical axis: 5v/div.

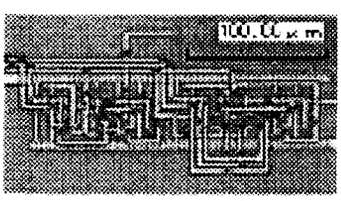

Fig. 12 Photomicrograph of fabricated C^2VSL half adder.

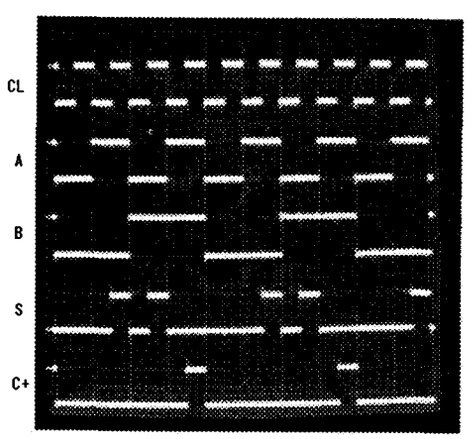

Fig. 13 Measured signal waveforms of C^2VSL half adder. Horizontal axis: 40μs/div. Vertical axis: 5V/div.

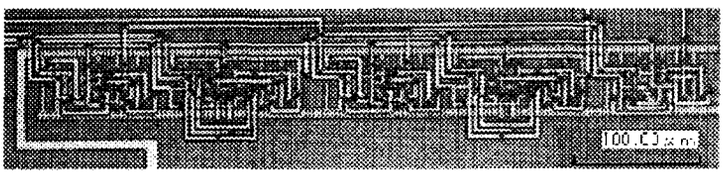

Fig. 14 Photomicrograph of fabricated C^2VSL full adder.

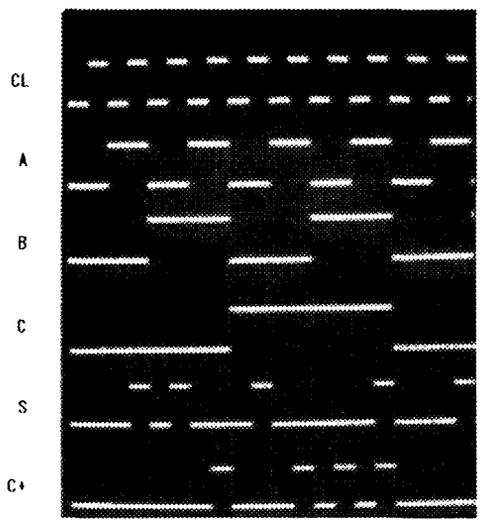

Fig. 15 Measured signal waveforms of C^2VSL full adder. Horizontal axis: 40μs/div. Vertical axis: 5v/div.

Fig. 4. Fig. 5 shows the C^2VSL half adder layout. Simulation results is shown in Fig. 6, indicating that the designed C^2VSL half adder functions correctly.

2.3 Clocked CVSL (C^2VSL) Full Adder

A C^2VSL full adder circuit diagram is shown in Fig. 7. Fig. 8 shows the C^2VSL full adder layout. Simulation results is shown in Fig. 9, indicating that the designed C^2VSL full adder functions correctly.

3. FABRICATION RESULTS

3.1 Static CVSL Half Adder

Fig. 10 shows photomicrograph of the fabricated static CVSL half adder. Measured signal waveforms of the static CVSL half adder is shown in Fig. 11, indicating that the fabricated static CVSL half adder functions correctly.

3.2 Clocked CVSL (C^2VSL) Half Adder

Fig. 12 shows photomicrograph of the fabricated C^2VSL half adder. Measured signal waveforms of the C^2VSL half adder is shown in Fig. 13, indicating that the fabricated C^2VSL half adder functions correctly.

3.3 Clocked CVSL (C^2VSL) Full Adder

Fig. 14 shows photomicrograph of the fabricated C^2VSL full adder. Measured signal waveforms of the C^2VSL full adder is shown in Fig. 15, indicating that the fabricated C^2VSL full adder functions correctly.

4. CONCLUSION

A static cascade voltage switch logic (CVSL) half adder, a clocked cascade voltage switch logic (C^2VSL) half adder and a C^2VSL full adder have been successfully designed and fabricated using a double polysilicon and double metal 1.2 μm CMOS technology. The three different adders have confirmed to function correctly by SPICE simulations. Furthermore, the fabricated three different adders have confirmed to function correctly by chip measurements.

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